CHAPTER 2

Dielectrics in Silicon Carbide Devices: Technology and Application

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Abstract

Formation of dielectric layers on SiC is a key feature of device processing technology. Achieving high mobility SiC MOSFETs is dependent on solving challenges within gate stack formation, where the dielectric plays a central role. Dielectrics also play a key role in surface passivation of SiC devices. This chapter reviews the main dielectrics that are used in SiC devices. The most commonly used dielectrics in electronic devices are SiO2 and Si3N4 and so these are introduced first, followed by high-κ dielectrics (i.e. dielectrics with higher permittivity than Si3N4). The methods of dielectric deposition are discussed before focusing on SiC thermal oxidation. Different parameters of the oxidation process and post-oxidation annealing, which have an impact on oxide quality and the formation of residual carbon in the SiO2/SiC interface, are evaluated. Efforts to improve electron mobility in SiC MOSFETs using a variety of dielectric layer formation techniques are reviewed, indicating where progress has been made. Issues surrounding SiC surface passivation by dielectrics are also discussed.

Keywords

Silicon Oxide, High-κ Dielectrics, MOSFET, Gate Oxide, Surface Passivation, Post Oxidation Annealing, Field Effect Mobility, Silicon Nitride

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List of used symbols and abbreviations

A  fitting parameter in Deal-Grove model of oxidation;
B  fitting parameter in Deal-Grove model of oxidation;
$C_{\text{dep}}$  depletion capacitance per unit area;
$C_{\text{GC}}$  gate-to-channel capacitance per unit area;
$C_{it}$  capacitive term per unit area associated with $D_{it}$;
$C_{ox}$  gate oxide capacitance per unit area;
$D_{it}$  density of interface traps;
$d_{ox}$  SiO$_2$ thickness;
$E_C$  conduction band minimum energy;
$E_{\text{eff}}$  effective electric field;
$E_g$  energy bandgap;
$E_i$  intrinsic Fermi level;
$F_{ox}$  dielectric strength;
$E_V$  valence band maximum energy;
$F_{1/2}$  Fermi-Dirac integral (of order 1/2);
$g_{d\text{i}}$  intrinsic channel conductance;
$g_{m\text{i}}$  intrinsic transconductance;
$I_D$  drain current;
$L$  gate length of MOSFET;
$n$  ideality factor in definition of the subthreshold;
$N_s$  density of charge carriers on the surface;
$N_{\text{depl}}$  depletion charge density close to an inverted SiC surface;
$q$  elementary charge;
$Q_{it}$  density of interface-trapped charge;
$Q_{\text{mobile}}$  density of mobile charge in the MOSFET channel;
$Q_n$  channel charge density;
$S$  subthreshold slope;
$T$ temperature;

$t$ time;

$V_{DS}$ source-drain voltage;

$V_{GS}$ gate-source voltage;

$V_t$ threshold voltage;

$W$ gate width of MOSFET;

$\beta$ current gain of BJT;

$\varepsilon_r$ relative permittivity (often referred to as dielectric constant);

$\eta$ weighting function for $N_S$ in definition of $F_{eff}$ depending on substrate orientation;

$\kappa$ relative permittivity (often referred to as dielectric constant);

$\mu_e$ charge carrier mobility contribution from Coulombic scattering;

$\mu_{eff}$ effective mobility;

$\mu_{FE}$ field effect mobility;

$\mu_i$ charge carrier mobility contribution from scattering at the SiC/\text{SiO}_2 interface (roughness);

$\mu_{inv}$ inversion layer mobility;

$\mu_p$ charge carrier mobility contribution from phonon scattering;

$\chi_{ox}$ oxide electron affinity;

$\psi_S$ surface potential;

3D three-dimensional;

ALD atomic layer deposition;

BJT bipolar junction transistors;

BSG borosilicate glass;

BTS bias temperature stress;

CMOS complementary metal oxide semiconductor field effect transistor;

CNL charge neutrality level;

CVD chemical vapor deposition;
DFT  density functional theory;
DLTS  deep level transient spectroscopy;
EELS  electron energy loss spectroscopy;
EOT  effective oxide thickness;
FINFET  fin field effect transistor;
HRTEM  high resolution transmission electron microscopy;
IGBT  insulated gate bipolar transistor;
LPCVD  low pressure chemical vapor deposition;
MIS  metal insulator semiconductor;
MOS  metal oxide semiconductor;
MOSCAP  metal oxide semiconductor capacitor;
MOSFET  metal oxide semiconductor field effect transistor;
NIT  near interface trap;
ONO  oxide/nitride/oxide;
PDA  post deposition annealing;
PECVD  plasma enhanced chemical vapor deposition;
POA  post oxidation annealing;
PSG  phosphosilicate glass;
RF  radio frequency;
SCM  scanning capacitance microscopy;
SIMS  secondary ion mass spectroscopy;
TDDB  time-dependent dielectric breakdown;
TEOS  tetraethyl orthosilicate;
TMA  trimethylaluminium;
UMOSFET  U metal oxide semiconductor field effect transistor.
XPS  x-ray photoelectron spectroscopy.
1. Introduction

Dielectrics are critically important materials used widely in semiconductor devices. They are used for electrical isolation between conductive elements, such as metal interconnections and semiconductors, as well as for passivation and protection of free semiconductor surfaces. Another important application of dielectrics is their use as the insulating layer in metal-insulator-semiconductor (MIS) capacitors, usually referred to as metal-oxide-semiconductor (MOS) capacitors (MOSCAPs) regardless of dielectric, and MOS field effect transistors (MOSFETs) [1]. The choice of an appropriate dielectric for specific application depends on its electrical properties, such as energy bandgap ($E_g$), critical electric field ($F_{ox}$, also known as ‘dielectric strength’), relative permittivity (also referred to as dielectric constant and designated here as $\varepsilon_r$ or $\kappa$) and electron affinity ($\chi_{ox}$), as well as on its chemical and mechanical compatibility with semiconductor device design and processing. These dielectric properties greatly influence the effective operation of semiconductor devices, such as their ability to withstand high electric field, high current density and high temperature. Different dielectrics applicable in SiC devices are discussed in this chapter.

The structural quality of a dielectric layer on a semiconductor is extremely important. For instance, in MOSFETs, the dielectric layer acts as an insulator between the gate contact and the channel, which is a thin (< 5 nm) semiconductor inversion layer at the semiconductor/dielectric interface, along which the flow of electrons is controlled by the gate voltage. The deposition or growth of a gate dielectric layer gives rise to defects located inside the dielectric and close to the dielectric/semiconductor interface. These defects can deteriorate device performance and reliability by reducing the dielectric strength and increasing gate leakage current.

1.1 Interface-trapped charge effects and requirements

The most important type of defect in MOS structures is interface-trapped charge. These defects are physically located at the dielectric-semiconductor interface and can include dangling bonds, Si-Si bonds, C-C bonds and various disorderly complexes created at the boundary between dielectric and semiconductor. These defects act as electrically available states, and electrons and holes can be captured and emitted. The density of interface traps charge per unit area and unit energy is given the symbol $D_{it}$.

When the interface traps are charged, the charge can decrease the channel conductivity due to Coulomb scattering of electrons. Furthermore, the active trapping and release of charge can further affect device performance. The capture and emission of electrons depends on the applied gate voltage, temperature and the initial trap state, and causes
instability in MOSFET operation and drift of its parameters. A semiconductor/dielectric interface always has some trapped charge, and it must be kept below certain limit. This limit can be estimated by recalling that the inversion layer surface charge density, $qN_s$, is given by:

$$qN_s = C_{ox} (V_{GS} - V_t)$$  

where $C_{ox}$ is the gate oxide capacitance per unit area, $V_{GS}$ is the gate voltage, $V_t$ is the threshold voltage, $q$ is the elementary charge and $N_s$ is the charge carriers surface density in the MOSFET channel. If the silicon dioxide (SiO$_2$) thickness ($t_{ox}$) is 100 nm and the gate overdrive voltage ($V_{GS} - V_t$) is 5 V then from Eq. 1 it is found that $N_s \sim 10^{12}$ cm$^{-2}$.

From Eq. 1, $N_s$ increases linearly as $V_{GS}$ increases or as $t_{ox}$ decreases. Ideally, $D_{it}$ needs to be lower than $10^{12}$ cm$^{-2}$, in the range $10^{10}$ - $10^{11}$ cm$^{-2}$, and the bulk density of electrically active defects in the SiO$_2$ below $10^{15}$ cm$^{-3}$ or below $4 \times 10^{-5}$ at.%. 

### 1.2 Near-interface trap effects

In addition to defect states physically located at the interface, charge can also become trapped in the dielectric. Some states will have constant, static occupancy, independent of gate voltage, and this trapped charge will contribute to shifts in flatband voltage for MOSCAPs and threshold voltage for MOSFETs. Some states, however, are capable of changing their occupancy. The nature, origin and effect of oxide states varies between material systems, a variety of descriptions are used and there is some disagreement among researchers regarding the topic.

For the 4$H$-SiC/SiO$_2$ system, the preferred nomenclature in the SiC/SiO$_2$ system is “near-interface traps” (NITs), although the term “border traps” is occasionally used, and they are observed to have an energy level close to the SiC conduction band edge [2]. Modelling using Density Functional Theory (DFT) has showed that CO molecules, C interstitials and C pairs can grow within the oxide, implicating them as the source of NITs [3]. Experiments using a thermally stimulated current technique have experimentally confirmed the presence of traps close to the conduction band edge of 4$H$-SiC [4]. $C-V$ and deep level transient spectroscopy (DLTS) measurements have found these traps centered 0.1 eV below the conduction band edge in 4$H$-SiC compared to 0.5 eV below the conduction band edge in 6$H$-SiC [5, 6].

NITs in the SiC/SiO$_2$ system have a very short time constant, trapping and releasing charge at least as fast as conventional interface-trapped charge. As such, their effect on device structures is generally lumped with conventional interface-trapped charge. NITs are not as widely studied as conventional interface-trapped charge, measured using $C-V$
techniques, but are important to improving channel mobility and have shown some response to changes in fabrication processes [7].

1.3 SiC MOS interface requirements

In general, trap states and trapped charge must be minimized in device structures. The main impediment to SiC devices is interface charge: both conventional interface-trapped charge, located physically at the interface, and near-interface traps, located sufficiently close to the interface to be electrically active. These affect the mobility of electrons in the channel, as detailed below in Section 2.1, but channel mobility is not the sole requirement of the SiC dielectric system.

The threshold voltage of MOSFETs can be influenced by fixed charge in the oxide and, for power applications, the target for threshold voltage is ~5 V to allow for easy operation but prevent accidental turn-on. Any alternative dielectric process must not drift further from this target than the incumbent process. Moreover, threshold voltage can be further influenced by trap states in the oxide, leading to instability over time and operation cycles. In addition to threshold voltage effects, DC leakage and dielectric breakdown are undesirable and should be controlled. In particular, deteriorating leakage performance over time and operation cycles has been observed in SiC MOS structures using time-dependent dielectric breakdown (TDDB) techniques [8, 9]. Leakage and leakage stability over time must also not be compromised by any alternative dielectric process.

These are specific cases of a general requirement: the dielectric must offer high reliability in addition to low $D_{it}$ and high channel mobility. Many dielectric processes discussed below offer improved channel mobility at the expense of reliability. The current incumbent technology is based on thermal oxidation – SiC is the only compound semiconductor that can be thermally oxidized to produce a SiO$_2$ layer, but the presence of carbon (C) atoms results in significant deterioration of the oxide quality, for all types of defect and trap state, in comparison to that grown on silicon (Si). For this reason, formation of SiO$_2$ layers on SiC requires tailored processes, unique from Si, such as post oxidation annealing (POA) or ultrathin interfacial oxides. Achieving a high-quality dielectric layer, with high structural quality and low interfacial charge, remains one of the main challenges in the development of SiC electronics. Different methods of dielectric deposition on SiC are reviewed in this chapter, alongside thermal oxidation.
2. Dielectrics in SiC device processing

2.1 Silicon dioxide in SiC devices

The success of Si electronics is in no small part due to the fact that a high structural quality SiO₂ can be readily grown on the Si surface by thermal oxidation. SiO₂ is used as the dielectric in SiC MOSFETs, as well as being a surface passivation layer and as a sacrificial layer in device fabrication. Unfortunately, the SiC/SiO₂ interface is poor compared with Si/SiO₂ and contains high levels of charged defects.

Electron mobility in the MOSFET channel is affected by several scattering processes, and by trapping processes. The scattering processes can be represented by Matthiesen’s rule:

\[
\frac{1}{\mu_{\text{inv}}} = \frac{1}{\mu_c} + \frac{1}{\mu_p} + \frac{1}{\mu_i}
\]  

(2)

The first term \(\mu_c\) corresponds to Coulomb scattering resulting from carrier-carrier interaction, electron scattering by fixed charges at the interface traps and remote scattering by charged defects in the SiO₂ or Si. The second term \(\mu_p\) corresponds with phonon scattering and is material dependent. The final term \(\mu_i\) corresponds with scattering due to the SiC/SiO₂ interface roughness in MOSFETs and dominates mobility at large gate voltages, \(V_{GS}\) [10]. These are combined to give the mobility for the inversion layer \(\mu_{\text{inv}}\).

Experimentally, field-effect mobility, \(\mu_{FE}\), is commonly used as a figure of merit for SiC MOSFETs. It can be calculated from MOSFET electrical measurements by [11]:

\[
\mu_{FE} = \frac{L g_m^i}{W C_{ox} V_{DS}}
\]  

(3)

In Eq. 3, \(g_m^i\) is the intrinsic transconductance [12], \(L\) is the gate length, and \(W\) is the gate width, \(V_{DS}\) is the source-drain voltage and \(C_{ox}\) is the gate oxide capacitance, measured using a split C-V configuration. \(\mu_{FE}\) is dependent on the electric field in the channel and, as a result, it is often plotted as a function of effective electric field, \(F_{eff}\), defined by:

\[
F_{eff} = \frac{q}{\varepsilon_0 \varepsilon_{\text{SiC}}} (N_{\text{depl}} + \eta N_S)
\]  

(4)

In Eq. 4, \(\varepsilon_{\text{SiC}}\) is the relative permittivity of SiC, \(N_{\text{depl}}\) is the depletion charge density close to the SiC surface, \(N_S\) is the inversion charge density, and \(\eta\) is the weighting function for \(N_S\) that depends on substrate orientation. For Si MOSFETs, \(\eta = 1/2\) for electrons on the (100) face, while \(\eta = 11/32\) is obtained theoretically [10]. Ohashi et al. [13] have shown that \(\eta = 1/3\) is a better fit to mobility data in C face SiC MOSFETs and this is expected to be the case for Si face SiC MOSFETs too.
Effective mobility, $\mu_{\text{eff}}$, is more commonly used as a figure of merit for Si MOSFETs. A plot of $\mu_{\text{eff}}$ versus $F_{\text{eff}}$ is known as a “universal mobility curve” because it is independent of substrate impurity concentration or bias. Effective mobility can be calculated from MOSFET measurements by:

$$\mu_{\text{eff}} = \frac{Lg^i_d}{WQ_n}$$  \hspace{1cm} (5)

In Eq. 5, $g^i_d$ is the channel conductance of the intrinsic device (e.g. when source/drain parasitics are removed). In an ideal MOSFET, free of interface charge, $Q_n$ is equal to the density of mobile charge in the channel, $Q_{\text{mobile}}$, which is calculated from the gate-to-channel capacitance per unit area, $C_{GC}$, according to [11]:

$$Q_{\text{mobile}} = \int_{-\infty}^{V_{GS}} C_{GC} dV_{GS}$$  \hspace{1cm} (6)

In the case of SiC MOSFETs, not all channel charge is mobile and so

$$Q_n = Q_{\text{mobile}} + Q_{it}$$  \hspace{1cm} (7)

where $Q_{it}$ is density of charge trapped at the interface. Trapped charge can be calculated from the measured $D_{it}$ by:

$$Q_{it} = q \int_{E_i}^{E_C} D_{it} F_{1/2}(E)dE$$  \hspace{1cm} (8)

In Eq. 7, $E_C$ is the conduction band minimum, $E_i$ is the intrinsic Fermi energy (i.e. the function integrates from $E_i$ to the conduction band edge) and $F_{1/2}$ is the Fermi-Dirac integral (of order 1/2). When substituted into Eq. 4, this can be summarized as:

$$\mu_{\text{eff}} = \frac{Lg^i_d}{W(Q_{\text{mobile}}+Q_{it})}$$  \hspace{1cm} (9)

Interface defects in SiC include impurities, features and decorations from bulk defect propagation. They may contribute to several mobility degradation processes: to Coulomb scattering as fixed or occupied charge states, to surface roughness scattering as points or regions of displacement and/or to trapping processes as variable-occupancy states. For the purposes of this chapter, the effect of interface degradation is considered as a lumped process, without distinguishing between different mobility degradation mechanisms.

4H-SiC, with a standard gate dielectric formed by thermal oxidation at around 1100 °C and without post oxidation annealing (POA) yields channel mobility values below 10 cm$^2/(V\cdot s)$ [14], compared to typical Si values > 200 cm$^2/(V\cdot s)$ [10]. On the other hand, bulk electron mobilities are of comparable magnitude in Si and SiC, being 900 cm$^2/(V\cdot s)$ for 4H-SiC and 1450 cm$^2/(V\cdot s)$ for Si. Therefore, the low electron
mobility in 4H-SiC MOSFETs is a result of poor interface quality between SiC and SiO$_2$. A large quantity of research over the last 20 years has looked at improving the electron mobility in SiC MOSFETs, for example, by reducing $D_{it}$.

SiO$_2$ can also be deposited by a variety of methods, as discussed in Section 3. Some combination of thermally grown and deposited SiO$_2$ can also be found in applications.

### 2.2 Silicon nitride in SiC devices

Silicon nitride ($\text{Si}_3\text{N}_4$) was investigated in the 1960s as an alternative dielectric to SiO$_2$ for the scaling of Si devices, because it has a higher permittivity. However, issues with interface quality and charge injection into the nitride made it an unsuitable choice for standard MOSFET technology. The oxide-nitride-oxide (ONO) structure was subsequently proposed for use in SiC power device technology, where it is desirable to employ a gate dielectric with a higher $\varepsilon_r$ than SiO$_2$, as SiC devices need to withstand high fields during operation compared with their silicon counterparts.

Lipkin and Palmour [1] have compared the reliability of a range of dielectrics (SiO$_2$, $\text{Si}_3\text{N}_4$, ONO, AlN) used on SiC for high voltage applications. While silicon oxides exhibited dielectric breakdowns at ~ 10 MV/cm, nitrides exhibited leakage current breakdown fields at ~ 5 MV/cm, which is related to the smaller electron affinity step using nitrides (1 to 2 eV) compared with oxides (~3 eV). ONO layers showed a combination of leakage and dielectric breakdown, with leakage current above 6.5 MV/cm. The breakdown field measured in MOSFETs is similar for oxide and ONO gate dielectrics, but the ONO thickness can be larger than the oxide and have the same capacitance, i.e. the same “effective oxide thickness” (EOT), thanks to the higher dielectric constant in the nitride.

The reliability performance of ONO was demonstrated to be equivalent to SiO$_2$ by time-dependent dielectric breakdown (TDDB) testing using ONO in a MOS capacitor, which consists of a bottom thermal oxide, LPCVD grown nitride and a pyrogenically oxidized top oxide with an estimated equivalent SiO$_2$ thickness of 40 nm [15]. Thermal oxide has been demonstrated to be superior to deposited oxide for the bottom oxide layer, but variations in nitride and top oxide formation have not been investigated. Further work using ONO structures showed the impact of underlying defects on the quality of thermal oxides and how the ONO structure can mitigate their impact [16]. ONO gate stacks have been incorporated into a normally-off MOSFET [17]. The ONO stack has been consistently shown to be a stable alternative to thermal oxidation and it can even be stressed reliably with a large negative bias, showing dielectric breakdown field strength of $-19.6$ MV/cm [18].
2.3 High-κ dielectrics in SiC devices

According to Gauss’s law, the product of permittivity and electric field normal to the dielectric/semiconductor interface has to be continuous. Therefore, for a given electric field in a semiconductor, the electric field in the dielectric can be lowered by replacing SiO₂ or Si₃N₄ with a dielectric that has a higher permittivity (κ). These high-κ dielectrics, such as HfO₂, Al₂O₃, BaTiO₃, TiO₂ and Ta₂O₅, have been of interest to the Si technology community because of their very high permittivities, and could potentially be of benefit to SiC technology in this regard. However, other material properties of high-κ dielectrics can mean that they are susceptible to leakage current and degradation, even at low electric fields, which detracts from their utility [1].

High-κ dielectrics have been used in CMOS logic technologies since the 45 nm node was introduced in 2007 [19]. To achieve the ever-higher drive currents required by Moore’s Law, these MOSFETs required ever-thinner gate oxides, which increases gate leakage by quantum mechanical tunneling. This leakage current can be minimized by using thicker layers of high-κ dielectrics that maintain the same capacitance and EOT, while increasing the gate oxide potential barrier to electrons. However, it is necessary to incorporate an ultrathin thermal SiO₂ layer prior to high-κ dielectric deposition, in order to reduce interface states to an acceptable level. The choice of high-κ dielectric also depends on there being a large enough electron affinity difference between the channel semiconductor and the gate dielectric to create a potential barrier to electrons in the gate dielectric and thereby minimize tunnel current.

SiC has a larger band gap than Si, so the potential barrier in the conduction band at the SiO₂/SiC interface is smaller. Consequently a larger tunneling current occurs than would be observed in an equivalent Si MOS gate stack with the same gate oxide thickness [8]. HfO₂, which has been used as a preferred high-κ material for Si technology, is not suitable for the SiC system due to a small electron affinity step (barrier height) at the HfO₂/SiC interface as shown in Fig. 1 [20, 21]. Therefore other high-κ materials that offer a wider bandgap and more favorable electron affinity step have been considered e.g. Al₂O₃ [21-25], LaSiOₐ [26] and AlN [27].

Among those materials, Al₂O₃ offers good performance in terms of gate leakage reliability and MOSFET channel mobility, but is not without problems. Tanner et al. [28] claimed that a deposited Al₂O₃ layer was crystallized by post deposition annealing (PDA) at 1100 °C. This reduced the electric field needed to generate a leakage current of 1×10⁻⁶ A·cm⁻² from 5 MV·cm⁻¹ to 1 MV·cm⁻¹. Additionally, Al₂O₃ suffers from trapping and de-trapping of electrons, a mechanism due to oxygen vacancies [29]. This results in hysteresis in MOSFET \( I_D-V_{GS}\) characteristics, which can be mitigated by
annealing during processing. Despite these issues, the maturity of Al₂O₃ technology and its integration with semiconductors results in it being commonly used in MOS structures.

For the formation of a good MOSFET gate stack, it is useful if there is a thin SiO₂ layer between the channel and dielectric layer to screen the remote scattering. The high-κ oxide layer should also be thin, so that the defect density is low, and so there are fewer traps that may otherwise contribute to \( I_D-V_{GS} \) hysteresis \([29]\). High-κ dielectrics must be deposited, and atomic layer deposition (ALD) is the preferred fabrication method for high-κ dielectrics, as discussed in Section 3.3.

3. Methods of dielectric deposition used in SiC device processing

Thermal oxidation of SiC produces a relatively poor SiC/SiO₂ interface in comparison with Si/SiO₂. Excess C is produced during oxidation that cannot incorporate into stoichiometric SiC or SiO₂ and so gives rise to C related defects close to the interface. These lead to a high density of interface states and hence a low channel mobility in SiC MOSFETs. One potential approach to mitigate against this is to deposit an oxide rather than consuming Si and C in thermal oxidation. SiO₂ may be deposited either by evaporation or by sputtering but these methods can only offer a “line-of-sight” deposited
film and so the layers are non-conformal [30]. The chemical vapor deposition (CVD) methods discussed below offer conformal coating, making them more common for fabrication of gate stacks and passivation dielectrics in SiC devices.

### 3.1 Plasma enhanced chemical vapor deposition of dielectric on SiC

CVD is the formation of a solid film on a substrate by the chemical reaction of vapor phase reactants that have the correct constituents. The reactants are introduced into a reaction chamber at a specific temperature to achieve required chemical reactions. Typical CVD processes for commonly used dielectrics in SiC technology, such as SiO$_2$, make use of silane (SiH$_4$) through the following reaction:

$$\text{SiH}_4 + \text{O}_2 \rightarrow \text{SiO}_2 + 2\text{H}_2 \quad (10)$$

Unlike conventional CVD, which relies on thermal energy to initiate and maintain chemical reactions, plasma enhanced CVD (PECVD) uses an RF induced glow discharge to provide energy to the reacting chemical species [30]. As a result, it enables higher deposition rates at lower temperatures. Desirable properties of PECVD films include reasonable electrical parameters, good long-term reliability, low pinhole count, good adhesion, good step coverage and conformity with underlying surfaces.

A glow discharge or plasma is created by an RF field applied to a low pressure gas, which creates free electrons. These electrons gain enough energy in the applied electric field that, when they collide with reactant gas molecules, the gas molecules decompose. These energetic chemical species are then adsorbed onto the surface where a film builds up. Improved film quality compared with thermal CVD processes is achieved because the chemical species (radicals) form stronger bonds to the surface and can more easily migrate along the surface. A potential problem with the use of these higher energy chemical species is poorer stoichiometry in the deposited films.

Some of the earliest studies on 6H-SiC claimed CVD SiO$_2$ quality to be as good as thermally grown oxide [31]. As SiC technology progressed and the problems with thermally grown gate oxides became clearer, PECVD deposited films, along with a suitable post oxidation anneal, were pursued and shown to give satisfactory interface state densities $\sim 10^{11}$ 1/(cm$^2$·eV) at 0.2 eV below the conduction band edge, resulting in lateral MOSFETs with mobilities over 50 cm$^2$/(V·s) [32-34]. For the CVD process, the most common implementation is PECVD with a deposition temperature of approximately 400 °C and with silane and O$_2$ as silicon and oxygen precursors, although other precursors (e.g. disilane, N$_2$O) can be used.
Masato et al. [35] compared an oxide thermally grown in N\(_2\)O to a PECVD deposited SiO\(_2\) with post oxidation N\(_2\)O and N\(_2\) anneal. The deposited oxide demonstrated a marginally better mobility at 26 cm\(^2\)/(V·s), compared to 20 cm\(^2\)/(V·s) for the thermally grown oxide. Moreover, the deposited oxide showed significant improvement in time-dependent dielectric breakdown testing, withstanding on average 70 C/cm\(^2\) of charge injected into the gate prior to breakdown, compared to 27.5 C/cm\(^2\) for the thermal oxide [35].

Another advantage of PECVD-deposited oxides is their thickness uniformity compared to thermal oxides for three-dimensional (3D) structures in SiC. For example, a trench in SiC, needed in the fabrication of UMOSFETs, will reveal different crystal planes. The SiC oxidation rate is different for different crystal planes, which will result in different thermally grown oxide thicknesses, while a conformally deposited PECVD oxide is of uniform thickness. PECVD has proved beneficial in the fabrication of 3D (or FINFET style) gate structures in 4H-SiC, which have 16× improved drain current density (compared to a planar device) due to the utilization of crystal planes with higher mobility [36].

### 3.2 Deposition of silicon oxide films using TEOS

Silane used for SiO\(_2\) deposition is pyrophoric – it ignites spontaneously on contact with air. A safer alternative precursor for SiO\(_2\) deposition is tetraethyl orthosilicate (TEOS), Si(OC\(_2\)H\(_5\))\(_4\), which is a colorless liquid that degrades in water:

\[
\text{Si(OC}_2\text{H}_5)_4 + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 4\text{C}_2\text{H}_5\text{OH}
\]  

(11)

TEOS is relatively inert and liquid at room temperature. Its vapor can be supplied to the reaction chamber by a bubbler and N\(_2\) carrier gas or by direct liquid injection. TEOS can be deposited via low pressure CVD (LPCVD) or PECVD. The chemical reaction for SiO\(_2\) deposition using TEOS at temperatures above 600 °C is:

\[
\text{Si(OC}_2\text{H}_5)_4 \text{(liquid)} \rightarrow \text{SiO}_2 \text{(solid)} + 2\text{C}_2\text{H}_4 \text{(gas)} + 2\text{H}_2\text{O} \text{(gas)}
\]

(12)

In the PECVD process, TEOS oxide can be deposited at lower temperatures (below 450 °C):

\[
\text{Si(OC}_2\text{H}_5)_4 \text{(liquid)} + \text{O}_2 \text{(gas)} \rightarrow \text{SiO}_2 \text{(solid)} + \text{other byproducts}
\]

(13)

Generally, deposited TEOS oxides have been used to passivate the SiC surface, or create field oxides, given the method has a high deposition rate and is well-suited to thick oxide films. It is not generally used as a gate oxide, as its breakdown electric field strength has
been shown [37] to be 60% of the equivalent oxide developed via a PECVD/silane process and the TEOS oxide also had 2-3× greater interface trap density. Another study [38, 39] reported an 8× improvement in channel mobility using a PECVD/TEOS oxide compared to counterparts with gate oxide formed by thermal oxidation (from 5 up to 40 cm²/(V·s)). However, these devices highlighted a key problem with TEOS layers as a gate dielectric, which is increased gate leakage. This is likely due to the quality of the TEOS dielectric, which can include pin holes, defects or trapped charge originating from dangling bonds. This often makes a densification process necessary after the TEOS oxide deposition to improve the layer’s stoichiometry [40].

Deposition of a gate oxide from TEOS has been combined with oxide doping by phosphorous to passivate the near-interface traps (phosphidation treatments are discussed in more detail in section 4.5). Lateral 4H-SiC MOSFETs fabricated by using this technique have demonstrated a channel mobility of 80 cm²/(V·s) [41].

3.3 Atomic layer deposition of gate dielectrics in SiC devices

Atomic Layer Deposition (ALD) is another method of depositing dielectrics on various substrates by utilizing a vapor phase technique. Owing to its sequential chemical process, the deposited layer thickness can be controlled to Angstrom level of accuracy with excellent conformality, even in high aspect ratio structures [42]. Deposition of high-κ dielectrics such as Al₂O₃ [43, 44] and SiO₂ [45] on SiC substrates have been reported. A schematic of a process for depositing Al₂O₃ on 4H-SiC is shown in Fig. 2. Initially, the 4H-SiC surface is terminated with a hydroxyl (OH) group following exposure to air as shown in Fig. 2a. Once the wafer has been inserted in the ALD chamber, a first chemical precursor, trimethylaluminium (TMA), is introduced. An ALD precursor will adsorb to and react with the 4H-SiC surface, producing a single uniform monolayer on the surface as depicted in Fig. 2b. Then the TMA and any by-product elements are pumped away before introducing water vapor in the chamber as shown in Fig. 2c. Now the water vapor reacts and replaces the CH₃ groups with OH groups. A further purge removes the remaining H₂O and CH₄ produced, leaving the surface terminated with OH groups. The cycle can then be repeated to grow a film of Al₂O₃ of desired thickness. During this process, the chamber pressure is kept at 600 mTorr with a temperature below 300 °C to prevent the surface from being oxidized. The precursors are transported to the reaction chamber by vapor draw with N₂ carrier gas. For ALD SiO₂ deposition on 4H-SiC, Yang et al. [45] used 3-Aminopropyltriethoxysilane, H₂O and O₃ as precursors, but ALD deposition of SiO₂ is not as mature as CVD processes and other precursors, such as bis(tert-butylamino)silane and bis(diethylamino)silane can be used.
Both ALD Al$_2$O$_3$ and ALD SiO$_2$ have been used as a gate oxide for 4H-SiC MOSFET fabrication. In 2009, Lichtenwalner et al. [23] reported a mobility of more than 100 cm$^2$/V·s in 4H-SiC MOSFETs using, as a gate dielectric, an ALD deposited Al$_2$O$_3$ with following post deposition annealing (PDA) at 400 °C for 30 s. Prior to the deposition of Al$_2$O$_3$, the samples were annealed in NO at high temperature for a short time to grow a SiO$_2$ layer and to control $D_{it}$.

Yang et al. [45] deposited 30 nm of SiO$_2$ by ALD and subsequently performed PDA in a nitrous oxide (N$_2$O) ambient. The highest electron mobility of 26 cm$^2$/V·s was achieved by performing PDA at 1100 °C for 40 s. The gate oxide could withstand effective fields up to 6 MV/cm within a leakage current range of $1 \times 10^{-7}$ A/cm$^2$. This value of maximum electric field is small compared to the thermally grown SiO$_2$, which can typically withstand up to 10 MV/cm. In other work, Yang et al. [26] inserted 1 nm of lanthanum silicate (LaSiO$_x$) between ALD deposited SiO$_2$ and 4H-SiC to form a gate stack. Peak mobility of 132.6 cm$^2$/V·s was found, with 3× larger current carrying capability compared to gate oxide without La$_2$O$_3$ but no $F_{ox}$ data was given.

Figure 2. ALD reaction cycle showing the growth of Al$_2$O$_3$ using TMA and water as precursors, with CH$_4$ as a by-product.
3.4 Densification of dielectrics deposited on SiC

As-deposited dielectrics are in general not lattice matched to the SiC substrate. They typically contain many defects and are more loosely packed than in their ideal crystalline state. In electrical terms, this means an uncontrolled increase in charge traps, which adversely affects electronic devices. Annealing such deposited dielectrics results in their densification and thereby improves their properties. The higher temperature of PDA allows the migration of constituent ions and the reduction of defect states in order to densify the dielectric.

$\text{Al}_2\text{O}_3$ is known to have quite a high defect concentration [29]. In particular the O vacancy has 5 stable charge states (+2, +1, 0, -1, -2) in the energy band gap, corresponding with four possible charge state transitions. If $\text{Al}_2\text{O}_3$ is used in the gate stack of a SiC MOSFET, the change in charge state of O vacancies changes the level of trapped charge in the oxide and so shifts the threshold voltage. As $V_{GS}$ is swept in either direction, charge state transitions occur at different points, giving rise to a hysteresis in the $I_D-V_{GS}$ curve, as shown in Fig. 3. Annealing performed immediately after the oxide deposition alleviates this problem [43].

3.5 Deposition methods conclusion

Deposition methods are of particular interest because no underlying substrate material is consumed and no carbon is incorporated into the oxide and interface. PECVD using silane offers high deposition rates, LPCVD and PECVD using TEOS can offer high deposition rates and good passivation, but require densification, and ALD offers excellent conformal coverage and fine control for low oxide thickness. Deposited dielectrics
benefit from PDA to improve oxide quality and/or interfacial layer formation to control $D_{\mu}$. In particular, ALD deposited Al$_2$O$_3$ contains high concentrations of oxygen vacancies as-deposited, and requires post-deposition annealing to control hysteresis – annealing processes are discussed in more detail in Section 4.5. Deposited dielectrics are not used commercially as gate oxides: PECVD and LPCVD are used for SiC field oxides and surface passivation (discussed in more detail in Section 6), whereas ALD is currently limited to academic research.

4. Thermal oxidation of SiC

SiC is the only compound semiconductor in which thermal oxidation results in the formation of a native oxide SiO$_2$. During the SiC thermal oxidation process, the volume of grown SiO$_2$ is equal to $2.16 \times$ the volume of SiC consumed, which is similar to the case of Si oxidation. In this section, we report first on the mechanics of SiO$_2$ growth on SiC by thermal oxidation and show the resulting oxidation rates. The problems and issues with these insulating layers are then discussed, given the presence of significant trapped C close to the interface [46].

4.1 SiC oxidation rates and a modified Deal-Grove model

For Si, the kinetics of thermal oxidation was modeled by Deal and Grove in 1965 [47] and this model is still an accepted approximation of ultimate oxide thickness, given process temperatures and times. The model assumes an initial layer of SiO$_2$ and that oxidation occurs at the Si/SiO$_2$ interface. Oxide growth is limited by the inward movement of the oxidant rather than the outward movement of Si. As laid out in the original work [47], the following three steps make up the kinetics of Si thermal oxidation:

1. a flux of oxidant species arrives at the oxide film’s outer surface;
2. it is transported across the oxide film towards the semiconductor;
3. it arrives at the semiconductor surface and reacts to form new SiO$_2$.

However, when considering the specific case of SiC, this simple case no longer holds true and one must factor in the removal of excess C. Given that:

$$\text{SiC} + 3/2 \text{O}_2 \rightarrow \text{SiO}_2 + \text{CO} \quad (14)$$

$$\text{SiC} + 2 \text{O}_2 \rightarrow \text{SiO}_2 + \text{CO}_2 \quad (15)$$

two more steps can be added to the above as follows [48]:

$$\text{SiC} + 3/2 \text{O}_2 \rightarrow \text{SiO}_2 + \text{CO}$$

$$\text{SiC} + 2 \text{O}_2 \rightarrow \text{SiO}_2 + \text{CO}_2$$
4. diffusional product gases (e.g., CO) through the oxide film;
5. removal of product gases away from the oxide surface.

In 2004, Song et al. [48], produced a modified Deal-Grove SiC oxidation model using these five steps as their starting point. The oxide thickness using this model is predicted as:

$$d_{\text{ox}}^2 + Ad_{\text{ox}} = Bt$$  \hspace{1cm} (16)

where $d_{\text{ox}}$ is the resulting SiO$_2$ thickness after an oxidation time $t$, $B$ is a parabolic rate constant and $B/A$ is a linear rate constant – these are derived in full in [48]. Subsequently, this model has been further improved [49] to better account for the early stages of oxidation. However, using Eq. 16, it is possible to approximate the oxidation rate for a number of temperatures, times and for different SiC crystal faces, as shown in Fig. 4. Oxidation on the Si face (0001) is slower than both the vertical a-plane (1120) by 6-10×, and the comparatively unused C face (0001). The vast majority of SiC devices use the long-established Si face, however, both the C face and the a-plane are of interest due to reports of high mobility on these surfaces, which shall be further discussed in Section 4.6.3. The a-plane can be exploited in SiC trench MOSFET architectures, while the C face of SiC has been used in the development of SiC IGBTs (insulated gate bipolar transistors) [50].

Figure 4. Left, oxide thickness as a function of time and temperature on the (0001) Si face of 4H-SiC. Right, oxide thickness as a function of time and SiC orientation on 4H-SiC, with Si oxidation as a reference. Reproduced from [48] with permission from AIP publishing.
4.2 Interface traps introduced during thermal oxidation of silicon carbide

As described in Eq. 14 and Eq. 15, unlike Si thermal oxidation, C is released during SiC thermal oxidation, for example as CO or CO$_2$ gases. However, in reality, a small amount of C remains close to the SiO$_2$/SiC interface according to the following reaction:

$$\text{SiC} + \text{O}_2 \rightarrow \text{SiO}_2 + \text{C}$$ (17)

What happens to the C remains the subject of some debate, though a wealth of evidence links the presence of carbon clusters to high interface state densities and hence low channel mobilities.

High resolution transmission electron microscopy (HRTEM) in Fig. 5a shows the existence of nm-scale transition layers at the SiC/SiO$_2$ interface [46, 51, 52]. For a 62 nm thermally grown SiO$_2$ layer, electron energy loss spectroscopy (EELS) data in Fig. 5b confirm a non-stoichiometric C/Si ratio extending 4 nm into the SiO$_2$ and 4 nm into the SiC. This can mean an excess of C or a deficit of Si in the SiC, or both. Specific defect identities cannot be assigned from this data but C interstitials, ternary SiO$_x$Cy phases and amorphous SiC are possible explanations. Graphitic features were detected using Raman spectroscopy on 4H-SiC surfaces following oxidation and etch [53], which could correspond to C clusters in SiC. Recently, rather than trying to mitigate the effects of excess C resulting from thermal oxidation of SiC to form a MOSFET gate stack, Arith et al. have minimized the formation of excess C by minimizing thermal oxidation of SiC [43]. They grew less than 1 nm of SiO$_2$ by low temperature (600 °C) oxidation. In this
way a field effect mobility of $125 \text{ cm}^2/\text{V} \cdot \text{s}$ was obtained in $4H$-SiC MOSFETs, indicating a high quality SiC/SiO$_2$ interface.

The C that resides at the interface between the SiC and the SiO$_2$ introduces trap states, with energy levels within the SiC bandgap. So-called “deep” interface traps have energy levels close to the middle of the SiC bandgap, which results in a net positive or negative charge at the interface. The polarity of deep interface traps depend on their energy relative to both the Fermi level and the charge neutrality level (CNL) of SiC, which has been simulated to be $1.71-1.85 \text{ eV}$ above the valence band for $4H$-SiC [54]. Gap state energies lower than the CNL, but greater than the Fermi level will act as ionized donors resulting in a net positive charge. Gap state energies greater than the CNL, but lower the Fermi level act as ionized acceptors resulting in a net negative charge.

Deep level traps are considered to have a major detrimental impact on the carrier lifetime of $4H$-SiC, particularly the Z$_{1/2}$ ($E_C - 0.65 \text{ eV}$) and EH$_{6/7}$ centers ($E_C - 1.55 \text{ eV}$) [55]. These can be largely reduced or suppressed via thermal oxidation at 1150–1300 °C, minimizing their impact on the SiC channel. However, this process has been shown, via deep level transient spectroscopy (DLTS) studies on oxidized $4H$-SiC, to result in a significant increase in the C interstitials related to the HK0 centre ($E_V + 0.78 \text{ eV}$) [55]. This hypothesis was reinforced by theoretical work identifying the HK0 as a di-interstitial of C that forms in the substrate after oxidation [56] that cannot be readily passivated by post oxidation annealing (POA). This deep level trap, it is concluded, is the likely cause of poor channel mobility of electrons in SiC MOSFETs.

In addition to the electrical action of residual carbon, it also results in increased interface roughness. As carbon tends to form clusters, rather than being distributed uniformly across the interface, interface roughness increases and mobility is degraded by interface roughness scattering as well as Coulomb scattering and carrier trapping. As discussed in Section 2.1, these effects are considered as a lumped process in this chapter.

Many approaches have been investigated to mitigate the effects of the presence of C. For example, re-oxidation where oxygen is supplied at a lower temperature after oxide growth to remove C clusters, i.e. CO molecules combine with oxygen and are moved away in the form of CO$_2$ [57, 58]. Argon annealing at 600 °C has also shown to be effective at reducing the presence of C clusters in the SiC/SiO$_2$ interface [59]. Other methods include the use of N containing gases, like N$_2$, NO and N$_2$O, either during oxidation or POA [60].

Similar to silicon technology, wet oxidation can give a much higher oxidation rate than dry oxidation. The increased oxidation rate significantly reduces control over the oxide thickness and uniformity. In addition, wet oxidation generates a high quantity of stacking
faults and surface pits, causing deterioration in SiO$_2$/SiC interface quality and oxide breakdown strength [61, 62]. Due to these issues, wet oxidation is not commonly used in SiC.

4.3 High temperature oxidation

In Si device technology, gate oxidation is typically performed at a temperature between 800 °C and 1000 °C. Thermal oxidation of SiC initially mimicked Si technology, but with an upper temperature limit of 1200 °C due to the slower rate of oxidation. Oxidation at 1300 °C was suggested to offer a decrease in C content and led to a lower $D_{it}$ [63]. MOS capacitors with thermal oxide grown at 1400 °C also showed a similar result [64]. The reason suggested was a higher oxidation rate of C than Si at these elevated temperatures, leading to faster removal of carbon atoms from the interface.

There has been evidence to suggest that using even higher temperatures, up to 1600 °C, may offer further benefit. This can be achieved using a conventional dry oxidation process in a tube furnace, itself made from SiC, rather than quartz, while some success has been demonstrated using rapid thermal oxidation [65]. A reduction in $D_{it}$ has been observed [66] for both 1500 °C and 1600 °C MOS capacitor structures formed via dry oxidation. For a lateral MOSFET structure utilizing a p-type epitaxial layer, a 1500 °C oxidation anneal produced a channel mobility of 40 cm$^2$/(V·s) [66]. It has also been highlighted [67] that, as well as a higher temperature being important, the final $D_{it}$ values are proportional to the flow rate of oxygen through the tube furnace, and hence minimizing flow rate can improve ultimate channel resistance. SIMS (secondary ion mass spectroscopy) and XPS (x-ray photoelectron spectroscopy) on thermally grown SiC/SiO$_2$ interfaces up to 1350 °C [68] have shown that those oxides grown in higher temperatures have a thinner transition layer of SiO$_x$ (0 < x < 1), which is suggested as the reason for reduced $D_{it}$ under these conditions.

Work on rapid thermal oxidation ranging from 1200 °C – 1700 °C has shown an optimum process temperature of 1450 °C for obtaining the lowest $D_{it}$ value [65]. 1700 °C is deemed unreasonably high as this is too close to the melting point of SiO$_2$ at 1710 °C. Cooling after the rapid thermal oxidation process, at any temperature, can result in unintentional oxide growth and shows the importance of gas flow control during but also after oxidation.

3C-SiC does not suffer as much as 4H-SiC in terms of channel mobility degradation due to its narrower bandgap, with fewer traps lying within it. One study [69] has shown it is also less sensitive to growth temperature, with a channel mobility of 70 cm$^2$/(V·s) achieved at oxidation temperatures of 1200 °C, 1300 °C and 1400 °C. Processing beyond
1400 °C is not possible due to 3C-SiC usually being epitaxially grown on a Si substrate [69].

### 4.4 Low temperature oxidation

Shen and Pantelides [56] suggested that immobile C di-interstitial defects \((C_i)_2\) are formed in SiC as a result of thermal oxidation. As already mentioned, defects of this kind may be responsible for the poor channel mobility observed in SiC MOSFETs. It can therefore be proposed to grow a thin SiO\(_2\) layer at low temperature as a route to decrease the density of these C related defects. This approach requires the additional deposition of a gate dielectric over the thin SiO\(_2\) layer to reduce the gate leakage current.

Hatayama et al. [25] measured peak mobilities as high as 300 cm\(^2\)/(V·s) in SiC MOSFETs utilising a 0.7 nm thick SiO\(_2\) gate dielectric grown at low temperature (600 °C) on SiC, followed by a deposition of Al\(_2\)O\(_3\) dielectric. They concluded that an interfacial oxide layer with thickness above 2 nm degrades the interface and channel mobility.

A field effect mobility of 125 cm\(^2\)/(V·s) and a subthreshold slope \((S)\) of 130 mV/dec were obtained by Arith et al. [43] in enhancement mode 4H-SiC MOSFETs with a channel length of 2 µm. This combination of high mobility, \(D_n\) levels in the range from \(6 \times 10^{11}\) - \(5 \times 10^{10}\) 1/(cm\(^2\)·eV) and low \(S\) is strong evidence of a good control of charged defects in the channel region [70]. \(S\) is the inverse gradient of the transfer characteristic, \(\log(I_D)\) versus \(V_{GS}\). Given the exponential dependence of \(I_D\) on \(V_{DS}\) in the subthreshold regime of MOSFET operation, \(S\) is given by:

\[
S = n \frac{kT}{q} \ln(10) \tag{18}
\]

where \(k\) is the Boltzmann’s constant, and \(T\) is the absolute temperature. For an ideal MOSFET \(n = 1\) and \(S = 60\) mV/dec. The ideality factor \(n\) in Eq. 18 can be written as:

\[
n = \frac{C_{ox} + C_{dep} + C_{it}}{C_{ox}} \tag{19}
\]

where \(C_{dep}\) is depletion capacitance per unit area and \(C_{it}\) is the capacitive term per unit area associated with \(D_n\) [11].

The devices were fabricated using an oxidation at 600 °C for 3 min in dry oxygen at atmospheric pressure [43]. The resulting oxide layer thickness was only 0.7 nm thick, thereby limiting the formation of defects in SiC following oxidation, and a 40 nm thick Al\(_2\)O\(_3\) formed by ALD. A high mobility was maintained over a wide gate voltage range, as shown in Fig. 6. The fabricated gate stack can also withstand electric field up to 6.5 MV/cm with a leakage current density of \(1 \times 10^{-6}\) A/cm\(^2\), thus indicating that this gate
oxide stack is robust. This work was extended by Urresti et al. [71] who demonstrated peak effective mobility of 265 cm²/(V·s) and device performance was shown to be up to 50% of that observed in Si MOSFETs, when compared by normalised universal mobility versus effective electric field as shown in Fig. 6b. The temperature dependence of field effect mobility revealed that coulombic scattering has been sufficiently reduced to make phonon scattering the dominant mechanism controlling carrier transport, further indicating that the use of a thin (0.7 nm) SiO₂ layer in the gate stack can control defects related to C that remain after oxidation. While these results are promising, at the time of writing there is no peer reviewed evidence whether the low temperature grown thin oxides suffer from $V_t$ instability or how stable they are in voltage or temperature stressing.

In addition, Kim et al. [72] have grown SiO₂ layers for MOS capacitors using direct plasma-assisted oxidation at room temperature. They claimed that the concentration of silicon oxycarbides (SiOₓCᵧ) is substantially reduced compared to thermally grown SiO₂ because the oxidation reaction mechanisms are different, and this leads to a reduced $D_u \sim 10^{11}$ 1/(cm²·eV).

Figure 6. (a) $I_D$–$V_{GS}$ transfer curve and field effect mobility by utilizing low temperature oxidation techniques. Reprinted, with permission, from [43] © 2018 IEEE. (b) effective mobility peaks at 265 cm²/(V·s) and device performance is up to 50% of that observed in Si MOSFETs as shown in a plot of mobility versus effective electric field. Reprinted, with permission, from [71]. © 2019 IEEE.
4.5 Post oxidation annealing

Performing POA in a particular gas ambient at temperatures of around 900 – 1400 °C after oxide formation is another method used to enhance oxide/4H-SiC interface quality and thus to improve electron mobility. One of the most promising POA methods is nitridation, which is employed in nitrogen rich gases such as nitric oxide (NO) [73, 74], nitrous oxide (N2O) [75, 76] or ammonia (NH3) [77, 78]. Chung et al. [73] demonstrated an improvement in electron mobility from single digits in MOSFETs using the as-grown oxide as a gate dielectric to 37 cm²/(V·s) in MOSFETs with the gate dielectric formed by thermal oxidation followed by POA in NO at 1175 °C for 2 hours [74]. During the nitridation process, nitrogen passivates interface traps by forming strong bonds with Si dangling bonds. In addition, the residual clustered C produced during thermal oxidation is also effectively removed [79, 80]. For example, a POA in NO at 1250 °C for 70 min [81], has been shown to reduce interface trap densities down to below 1×10¹² 1/(cm²·eV). A correlation between N concentration and electron mobility was reported by Rozen et al. [82, 83], who showed that interface trap density decreased and peak mobility increased as a function of nitridation time. A minimum trap density was achieved after 4 hours in NO at 1175 °C, resulting in a mobility of 45 cm²/(V·s).

POA in N2O is widely used as an alternative solution because NO gas is highly toxic [75]. Jamet et al. [84] revealed that POA with either NO or N2O produced an almost identical effect at the interface, due to the fact that N2O decomposes into NO gas at a temperature of around 1200 °C [8, 85].

Another effective technique to reduce interface traps and enhance electron mobility is to perform POA in POCl3 [86]. Peak mobility as high as 89 cm²/(V·s) was achieved in MOSFETs with thermally grown gate oxide annealed in POCl3 at 1000 °C. This mobility level was further improved to 101 cm²/(V·s) with multistep POCl3 annealing [87]. The conversion of thermally grown SiO₂ into phosphosilicate glass (PSG) during POCl3 annealing can be attributed to the suppression of interface traps and an improvement of channel mobility [7]. Jiao et al. [88] reported that the percentage of phosphorus uptake at the PSG/SiC interface within the channel region depends on the POCl3 annealing temperature. The lowest value of Dₜ was achieved after POA in POCl3 at 900 °C, the lowest temperature tested. However, PSG gate oxide has a polarization effect and thus a gate instability issue arises with higher phosphorus uptake at the interface [88]. One of the main reasons for this is the presence of oxide traps in the PSG and near the interface traps [24].

POA in boron gas is another alternative to passivate interface traps and improve electron mobility in the 4H-SiC MOSFET. By a similar mechanism to that with PSG, thermally
grown SiO₂ is converted to borosilicate glass (BSG) by a two-step annealing process. A mobility of 102 cm²/(V·s) has been obtained with a low $D_{it}$ value of $9.0 \times 10^{11}$ 1/(cm²·eV) [89]. Boron atoms were uniformly distributed in the oxide and effectively passivated the active interface traps. The improvement in electron mobility has been suggested to be due to stress relaxation in the SiO₂ structure [89]. Recently, Cabello et al. [90] reported peak electron mobility as high as 160 cm²/(V·s) with a nitrided gate oxide followed by boron annealing. Relatively good $V_t$ control was observed under positive and negative bias stress instability testing at room temperature with a boron annealed gate oxide [90].

4.6 Thermal oxidation conclusion

SiC benefits from being the only compound semiconductor with a stable thermally-grown oxide (SiO₂), but the residual carbon from the oxidation process significantly impacts on thermally-grown oxides. Some carbon escapes as CO and CO₂, but some remains as graphitic carbon clusters at the interface and contributes significantly to $D_{it}$ and mobility degradation. Oxidation at higher temperature and with low oxygen flow rate can mitigate the formation of carbon clusters, promoting the formation of CO and CO₂, but is limited by the melting point of quartz chambers and the SiC itself. High-quality thin interfacial layers can be formed with low temperature oxidation, producing a foundation structure for a deposited dielectric. Post-oxidation annealing (POA) offers further opportunities to passivate residual carbon: phosphorus-based and boron-based processes have demonstrated the highest channel mobility, but nitrogen-based processes offer good channel mobility and excellent stability and reliability. The preferred POA process is nitridation, using NO or N₂O.

5. Other methods to improve channel mobility

5.1 Sodium enhanced oxidation

Sodium enhanced oxidation is a method to improve channel mobility where sodium (Na) is present in the furnace during thermal oxidation [91]. A mobility up to 170 cm²/(V·s) was reported [92], the result of Na ions increasing the oxidation rate and reducing the formation of interface traps [93]. However, mobile Na ions can diffuse into the gate oxide and cause instability in threshold voltage, and this behaviour has been well recognised in Si technology [70]. Lichtenwalner et al. [94] reported the use of group I alkali elements Rb and Cs and group II alkaline earth elements Ca, Sr and Ba as interface passivation materials prior to thermal oxidation of the MOSFET channel region. Those MOSFETs with gate stacks consisting of an ultrathin layer of Ba (~ 0.6 - 0.8 nm) and 30 nm of deposited SiO₂ produced a mobility of 85 cm²/(V·s). This technique also results in a
reduction in $D_n$ close to the conduction band compared to thermally grown gate oxide and NO treated gate oxide. Unlike Na-contaminated gate oxide, which contains a large number of mobile ions, the Ba interlayer gate stack demonstrated a consistent threshold voltage with a slight hysteresis of 0.8 V during positive bias temperature stress (BTS) measurements. This suggests that the Ba atoms are less mobile, and hence become strongly bonded and effectively passivate the interface traps.

5.2 Counter doped channel regions

Counter doped MOSFETs have been investigated by implanting group-V elements into the channel region of n-channel MOSFETs. This technique was first introduced by Ueno et al. [95] who implanted nitrogen ions into the SiC channel region prior to the formation of the gate oxide. Channel mobility increased and the threshold voltage decreased with increasing nitrogen dose [95]. Instead of direct implantation, interface doping in the channel region can also be formed by POA. Fiorenza et al. [96] observed the heavily doped nitrogen and phosphorus atoms at the channel after POA in N2O and POCl3 using a Scanning Capacitance Microscopy (SCM) probe [96]. The SCM probe also detected an electrically active region underneath the deposited SiO2.

Counterdoping the channel region of a MOSFET with antimony (Sb) prior to thermal oxidation and NO annealing is a process that resulted in a mobility of up to 110 cm²/(V·s) [97]. Zheng et al. [98] later reported that by replacing the standard NO POA after the Sb treatment with a POA in O2 at 950 °C for 30 min with a B2O3 planar diffusion source, a mobility of 180 cm²/(V·s) was achieved. However, the borosilicate glass (BSG) gate exhibited a high threshold voltage hysteresis of up to 8 V at 1.5 MV/cm stress at 150 °C during the BTS measurement [98]. The poor BTS performance was suggested to be due to the large concentration of oxide traps, which is a characteristic of BSG gate oxide [99].

5.3 Alternative SiC crystal faces

The Si face (0001) of 4H-SiC, though the most commonly used and most well characterized, has a slow oxidation rate and a low channel mobility. Pictured in Chapter 1 of this volume in Fig. 3 are alternative crystal planes, which have been shown to have lower interface state densities, and higher mobility than the Si face. These include the a-plane (1120), which is commonly used for vertical channels in the formation of trench MOSFETs, and C face (0001), which is being used in the formation of SiC IGBTs [50].

4H-SiC MOSFETs formed on the a-plane exhibited a field effect mobility of 85 cm²/(V·s) after conventional NO passivation [100]. Using a PSG treatment instead of NO, this reached 125 cm²/(V·s). Research benchmarking the mobility of the a- and m-planes and the Si face after NO treatment at 1300 °C for 80 min demonstrated that the a-
plane has a peak channel mobility of up to 108 cm²/(V·s), compared to 46 and 37 cm²/(V·s) for the C and Si faces, respectively [101]. The authors show that a high channel mobility was observed for the a-plane regardless of nitridation conditions, be it using NO or N₂O [101]. However, oxide thickness varies on each crystal face due to different growth rates and hence must be precisely controlled to guarantee a $V_t$ value.

The Si face has shown poor response to wet oxidation and H₂ annealing. However, the a-plane and C face have shown low $D_{it}$ and high channel mobility following wet oxidation and H₂ anneal. Channel mobility greater than 100 cm²/(V·s) has been obtained after wet oxidation and H₂ POA, with wet oxidation alone showing higher mobility than dry oxidation alone for these faces and H₂ POA showing further improvement [102, 103]. On the a-plane and C face, this combination of wet oxidation with H₂ POA gives higher channel mobility and lower $D_{it}$ than dry oxidation with nitridation, and gives higher channel mobility than either process on the Si face. A summary of $\mu_{FE}$ and $D_{it}$ for these process/plane combinations is shown in Fig. 7 [104].

6. Surface passivation by dielectrics

The development of high voltage power devices necessitates a passivating layer to dissipate the electric field at the semiconductor surface. SiO₂ is the natural material choice for surface passivation, when grown by thermal oxidation of the SiC substrate. As with thermally grown SiO₂ for the gate stack, post oxidation anneals improve electrical performance but not to the extent of silicon [105, 106].
The impact of interfacial charge on the design of termination structures for SiC power devices of all types is of importance. Interface charge will lead to increased leakage current when the device is in the blocking state, though this can be reduced using POA treatments [107], as in the MOS interface. In the case of using a bevel-edged termination structure, it has been shown [108] that implanting the surface with argon can create a highly resistive area beneath the passivation region, reducing the field at the surface.

For bipolar devices, charge at the SiC/SiO$_2$ interface increases surface recombination [109, 110], which will affect carrier lifetime and the current gain ($\beta$) of bipolar junction transistors (BJTs) [109]. The passivation of SiC BJTs, which will include sidewall passivation of emitter/base mesa structures, is strongly affected by the density of interface traps present at a grown SiC/SiO$_2$ interface. On the sidewall of a BJT emitter/base region, these cause electrons to recombine at this interface, degrading emitter injection efficiency, and hence gain [109, 111, 112]. The impact of passivation oxide thickness on BJT gain has been demonstrated also [113], with a passivating layer of 100-150 nm delivering 60% greater gain ($\beta > 200$) compared with thinner 50 nm passivation. The gain can be traded off in further bipolar design to improve other electrical parameters.

Polyimide is used extensively in the electronics industry for surface passivation [114]. A thick layer of polyimide has been evaluated as the passivation for high voltage Schottky [115] and PiN [116] diodes, and compared to thick deposited SiO$_2$ layers. In the case of the PiN diode, after 40 nm of thermal oxide was formed on the surface of the JTE, a 4 µm polyimide layer was used as a second passivating layer. This resulted in a breakdown voltage that was on average 25% higher than when a 1.8 µm SiO$_2$ layer was used as a second passivating layer. However, the difference in thickness of these layers is substantial, leaving the benefit of polyimide compared to reported thick PECVD SiO$_2$ depositions unclear [117].

7. Summary

The focus of this chapter has been around the impact of dielectrics on the performance of SiC devices and, in particular, 4H-SiC MOSFETs. Fig. 8 shows the current status of (field effect) mobility as a function of $D_{it}$ at 0.2 eV near to the conduction band edge, covered in this review. To date, encouraging improvements have been achieved in increasing channel mobility in 4H-SiC MOSFETs. However, the value of peak channel mobility of 4H-SiC MOSFET is still behind that achieved by silicon MOSFETs. Fig. 8 shows that the field effect mobility is inversely proportional to $D_{it}$, indicating that interface state traps contribute to the limiting of electron mobility. The correlation in the
data is somewhat weak, which may result from different device specifications and/or electrical characterization parameters. Nevertheless, the best performing MOSFETs lead to data towards the top left corner of Fig. 8, corresponding with high mobility and low $D_{it}$. Fig. 8 shows that POA in N-rich gases does not improve mobility as well as POA in B or P gases. However, there are issues with $I-V$ hysteresis in devices using B or P gases, resulting on N-rich gases being preferred, despite lower channel mobility. The use of thin interfacial layers offers significant improvements in device performance, using low temperature oxidation followed by dielectric deposition.

Mobilities in excess of 100 cm$^2$/(V·s) have been achieved via a number of different techniques, in particular by the use of high-κ dielectrics, thin thermal oxides or the use of alternative crystal planes. POA and high temperature oxidation has also been shown to improve mobility, although to a lesser extent using N-rich gases.

Despite improvements in channel mobility, new processes have not supplanted thermal oxidation and POA in NO or N$_2$O, principally because of compromises in leakage current, threshold voltage stability, hysteresis and general reliability. The importance of controlling residual C close to the SiC/SiO$_2$ interface has been stressed, and factors that mitigate its effect have been discussed.

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